Design of Point Processing Algorithm using Hardware Co-simulation for Digital Image Processing Application

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Abstract — **Image processing is one an important application which has a strong mathematical basis. It is always one of the classical Studying projects of computer vision and image processing field. Application areas of signal processing have increase in recent year, in parallel with the growth of powerful and low-cost processing chips. In this paper we are using point processes which are only the information in individual pixels to produce new images. Arithmetic operations, XOR operations, histograms, contrast stretching and intensity transformations are implemented using Xilinx System Generator (XSG). XSG is a useful tool to understand fundamental Digital Signal Processing (DSP) algorithms for Field Programmable Gate Array (FPGA) implementation. In this paper FPGA-based architecture for Point Processing algorithms has been proposed. FPGAs are providing a platform for processing real time algorithms on application-specific hardware with substantially higher performance than programmable digital signal processors (DSPs).**

Keywords- **FPGA, Image Processing, Point Processing, Xilinx System Generator**

I. INTRODUCTION

In recent years, with the rapid development of economic, the process of town urbanization developed continuously, and land-use has becoming a community-wide hot issue. The construction land becomes increasingly tense and getting greater pressure. Therefore, extracting the current building Information from high resolution image and getting the current land use has provided a guarantee for rational planning and utilization of land resources in villages and towns. With the rapid development of remote sensing technology, we can choose the present application of the high resolution remote sensing image. The emergence of digital aerial camera solves the problem of the low productivity of traditional image and the poor real-time photographing [1].In this paper, we study digital images and its processing techniques, specifically point processing algorithms. FPGA [2] is a form of highly configurable hardware while DSPs are specialized form of microprocessors. System Generator [3] is the modeling tool in which designs are captured in the DSP friendly Simulink modeling environment using Xilinx specific Block set.

Point processes are the simplest and basic image processing operations. They operate on a pixel bases solely on that pixel's value. Although point operations are the simplest, they contain some of the most powerful and widely used of all image processing operations. They are especially useful in image pre-processing, where an image is required To be modified before the man job is attempted. Important point Processing operations are arithmetic operations, XOR operations, histograms with equalization, and Contrast stretching and intensity transformations along with the implementations which are done using XSG.

II. LITERATURE REVIEW

Lot of work done on Point Processing Algorithm .On the basis of that algorithm, we can improve quality of image & solves the problem of the low productivity of traditional image and also the poor real-time photographing

[R.Harinarayan,R.Pannerselvam, M.Mubara Ali, Dhirendra Kumar Tripathi] implemented two different methodologies for the edge detection of aerial images implemented on the FPGA. Lower requirements of the FPGA resources make this method easy to be integrated with the aerial surveillance instruments and automatic navigation equipments [4]

[Neha. P. Raut,Prof.A.V.Gokhale] proposed Image Processing Algorithms using the most efficient tool called Xilinx System Generator (XSG) for Mat lab [5]

[V. Elamaran, G.Rajkumar] Proposed a real-time image processing algorithms implemented on FPGA Advances in FPGA technology with the development of sophisticated and efficient tools for modeling, simulation and synthesis have made FPGA a highly useful platform.[6]

[Alba M.Sanchez G, Richardo Alvarez G, Sully Sanchez G, FCC and FCE BUAP] implemented architecture and a hardware efficient FPGA based watermark module towards the development of the complete digital camera. [7]

III. PROPOSED WORK

The entire operation will propose using Simulink and Xilinx blocks goes through three phases & these are

- Image pre-processing blocks.
- Edge enhancement algorithm using XSG.
- Image post-processing blocks

The design flow of hardware implementation of point processing operation using XSG is given in fig 1.Image source and image viewer are simulink block sets by using these blocks image can give as input and output image can be viewed on

image viewer block set. Image pre-processing and image post-processing units are common for all the image processing applications which are designed using Simulink block sets.

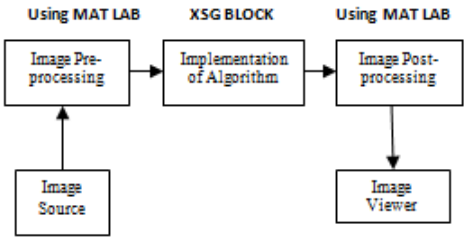

Fig 1: Design flow of hardware implementation of point processing operation

A. *Image pre-processing blocks:*

Image pre-processing in Mat lab helps to provide input to FPGA as specific test vector array which is suitable for FPGA Bit stream compilation using system generator.

• Resize: Resize block set input dimensions for an image.

• Convert 2-D to 1-D: image is converted into single array of pixels.

• Frame conversion and buffer: It is used to setting sampling mode and buffering of data.

B. *Image post processing blocks*:

Image post processing helps to recreate image from 1D to 2D

- Data type conversion: Data type conversion converts image signal to unsigned integer format.
- Buffer: Buffer converts scalar samples to frame output at lower sampling rate.
- Convert 1D to 2D: Convert 1D image signal to 2D image matrix.
- Sink: Sink is used to display the output image back on the monitor.

This paper contain the fundamentals of all point processes in image processing and shows the simulation results using Xilinx System Generator for the models designed.

C. *Algorithm for Color Image Brightness.*

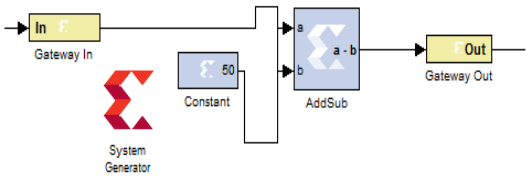

Fig 1: XSG block for Addition

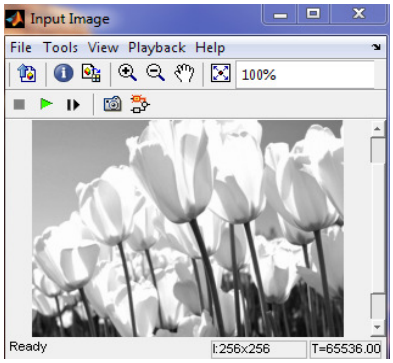

Fig 2: Original Image

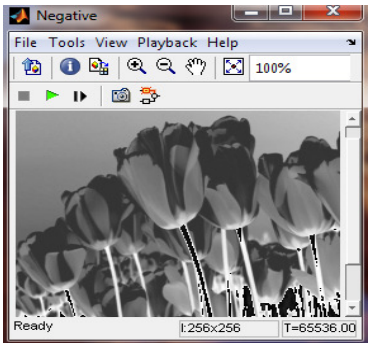

Fig 3: Image+50

C. *Algorithm for Colour Image Inversion.*

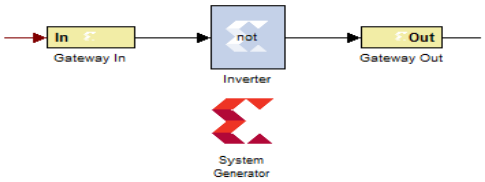

Fig 4: XSG block for Inversion

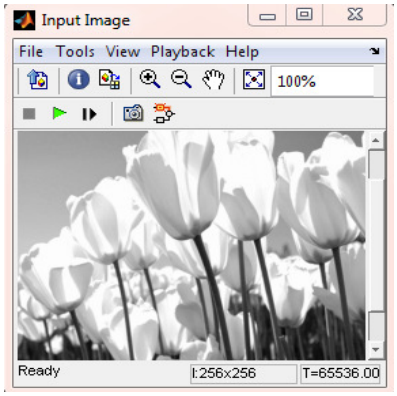

Fig 5: Original Image

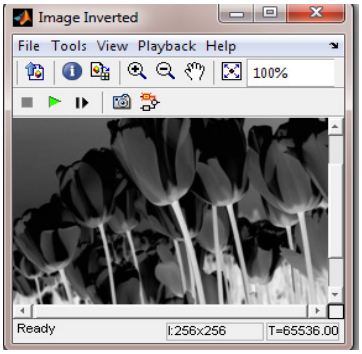

Fig 6: Image Inverted

IV. SIMULATION RESULTS

The hardware implementation results are produced using Xilinx Spartan 6 FPGA. The Simulation Result for Brightness Control (Device Utilization Summary) is shown in table.

Slices	1	Out of 4656
Flip flops	1	Out of 9312
IOBs	26	Out of 232
CLKs	1	Out of 24

Table: Device Utilization Summary

V. CONCLUSION

The implementation of point processing algorithms using Xilinx System Generator will extended to applications like background estimation in video, image filtering & digital image watermarking applications, etc. The implementation will reduces cost of Instrument, reduces its Complexity & also Time.The result given in this work proves that the proposed hardware implementation of point processing operation gives optimal result for all kind of images which is used for various applications

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