High Speed Convolution and Deconvolution Algorithm based on Ancient Indian Vedic Mathematics

Dr. Ujwala A. Belorkar **Mr. Ashish E. Bhande**

Abstract - **Convolution and deconvolution provides the mathematical framework for Digital Signal Processor(DSP). They are the most important techniques in Digital Signal Processing. but Both operation consume much of time.So our focus to develope more advance and simpler techniques. This paper presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution.The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The implementation of linear convolution and circular convolution using vedic mathematics is functionally verified using Modelsim software and analyze on Altera FPGA platform using Quartus 2 software, parameter like area, speed and power will be compared to their implementation using conventional multiplier & divider architectures.**

Index Terms— Convolution, Deconvolution, Vedic Mathematics, VHDL

I. INTRODUCTION

With the latest advancement technology, digital signal processing plays a pivotal role in many areas of electrical engineering.

Convolution and deconvolution are central to many applications of Digital Signal Processing and Image Processing.These are frequently used operation in DSP .However, beginners often struggle with convolution and decovolution because the concept and computation requires a number of steps that are tedious and slow to perform. For engineers ,complexity and excess time consumption are always the major concern which motivates us to focus on more advance and simpler techniques .Therefore many of researchers have been trying to improve performance parameters of convolution and deconvolution system using new algorithms and hardware.

Vedic Mathematics provides unique solution for this problem. Many engineering application areas use this Vedic Mathematics, especially in signal processing. It has 16 sutras and sub-sutras which cover all the branches of mathematics such as arithmetic, algebra, geometry, trigonometry, statistics etc. Implementation of these algorithms in processors has found out to be advantageous in terms of reduction in power and area along with considerable increase in speed requirements.These Sutras are given in Vedas centuries ago. To be specific, these sutras are described in ATHARVA-VEDA. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic M Ancient Indian.

Vedic Mathematics sutras, Urdhva Triyagbhyam or Vertically and Crosswise Algorithm for multiplication is discussed and then used to develop digital multiplier architecture. For division, different division algorithms are studied, by comparing drawbacks and advantages of each algorithm, Nikhilam Algorithm based on vedic mathematics is modified according to need and then used.

II. BACKGROUND WORK

In [1] Surabhi Jain and Sandeep Saini presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures.In [2] Madhura Tilak presents a novel method of implementing linear convolution of two proposed method uses modified design approach by replacing the conventional multiplier by Vedic multiplier internally in the implementations. The proposed method is efficient in terms of computational speed, hardware resources and area significantly. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches.The proposed circuit is also modular, expandable and regular which provides flexibility. In [3] Mrs.Rashmi Rahul Kulkarni ,convolution is carried out by serial processing. They used only one 4×4 bit Vedic multiplier based on Urdhva Tiryagbhyam sutra. Though hardware is less, delay is more as sixteen multiplications are carried out one by one using only single multiplier. In this paper, convolution of two finite length sequences is computed using Direct method. This method is similar to the multiplication of two decimal numbers, this similarity that makes this method easy to learn and quick to compute. As Vedic multiplier is high speed multiplier among existing multipliers, Urdhva Tiryagbhyam algorithm from Vedic mathematics is used for 4×4 bit multiplication and to improve speed parallel processing approach is used. In [4] Rashmi K. Lomte (Mrs.Rashmi R. Kulkarni), Prof.Bhaskar P.C proposed deconvolution of two finite length sequences (NXM) using direct method to reduce

deconvolution processing time. In this paper, we presented an optimized implementation of deconvolution. This particular model has the advantage of being fine tuned for signal processing. To accurately analyze our proposed system, we have coded our design using the VHDL hardware description language and have synthesized it for FPGA products using ISE. The proposed circuit uses less area and less power.

III. SYSTEM DESCRIPTION

System describes, Vedic mathematics sutra urdhva triyagbhayam and nikhilam algorithm.
Urdhva Triyagbhyam Sutra:

Vedic mathematics contains sutras (formulas) which are simple and straightforward, even though they are based on algebra, these sutras work like magic and unlike modern algebraic formula, they are easy to remember.More importantly, vedic mathematics means almost zero paper work.The conventional method for multiplication is very complicated and, as the number of digits increases, the method gets more and more complicated, involves more paper work, is more elaborate, takes more time to solve, is more prone to human errors while adding, placing digits one below other etc. Now let us see how simple it is to do the same arithmetic using the vedic mathematics sutra Urdhva Tiryagbhyam i.e vertically and crosswise.

Three digit multiplication

The urdhva Tiryagbhyam method for 3 digits is as follows,

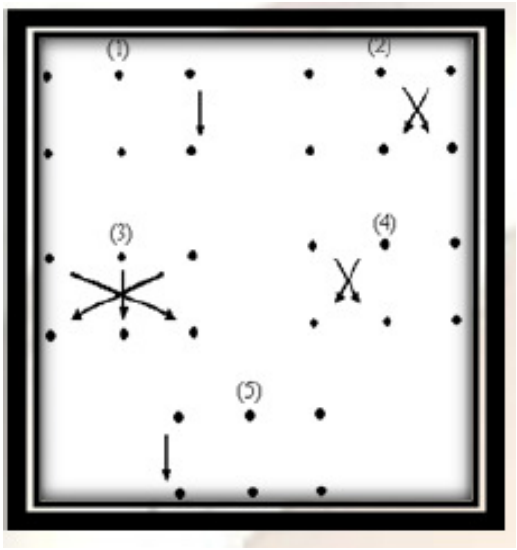

Fig.1

Similarly for any number of digits this multiplication technique of ancient Indian Vedic mathematics can be used.

Vedic Divider: Nikhilam Algorithm: Nikhilam Navatascaramam Dasatah, literally meaning all from 9 And the last from 10. In this algorithm following steps occur.

Breaks up the dividend into two parts.

Adjusts the divisor by complimentingitusing the procedure "subtract all from 9 and the last from 10" .

Next, the first digit of the quotient part is divided by the first digit of the actual divisor.

In this step, the remainder from the previous step is first written as the most significant digit of the quotient part and then it is multiplied by the adjusted divisor and placed below the dividend after shifting it one place right and perform the addition..

The basic work proposed in this paper is been explained using the block diagram in Fig 2.

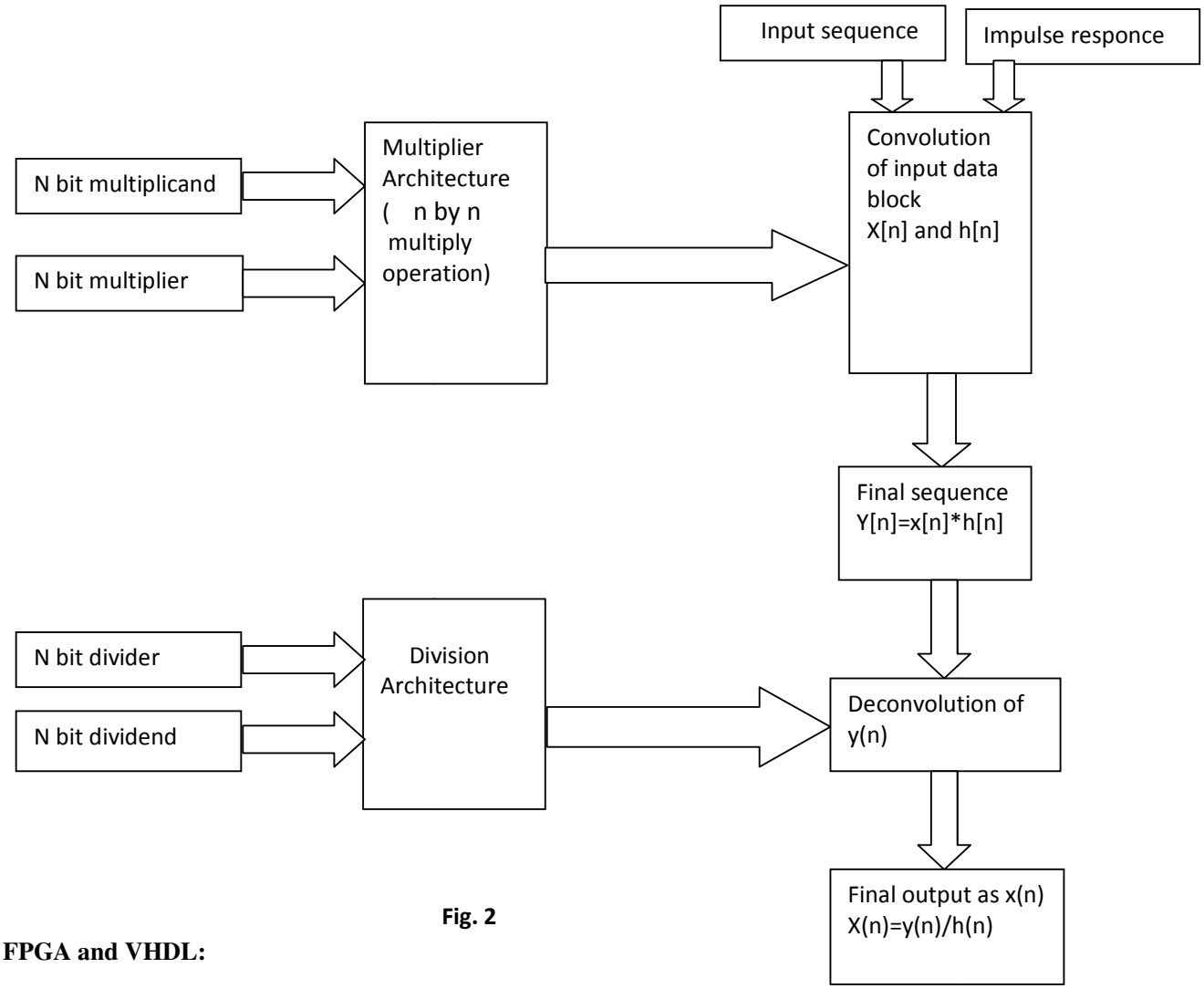

Fig. 2

FPGA and VHDL:

FPGA or Field Programmable Gate Arrays can be programmed or configured by the user or designer after manufacturing and during implementation. FPGAs can be used to implement any logical function that an ASIC can perform. It can be programmed or configured by the user or designer after manufacturing and during implementation. Hence they are otherwise known as On-Site programmable. Unlike a Programmable Array Logic (PAL) or other programmable device, their structure is similar to that of a gate-array or an ASIC. Thus, they are used to rapidly prototype ASICs, or as a substitute for places where an ASIC will eventually be used.

FPGAs have become very popular in the recent years owing to the following advantages that they offer: They are Fast prototyping and turn-around time, NRE cost is zero, High-Speed, low cost. To programme FPGA one should have knowledge of HDL language. That may be VHDL or Verilog. Its concept can be explained well as below.

VHDL is an acronym for VHSIC Hardware Description Language (VHSIC is an acronym for Very High Speed Integrated Circuits). It is a hardware description

language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level. The complexity of the digital system being modeled could vary from that of a simple gate to a complete digital electronic system, or anything in between. The digital system can also be described hierarchically. Timing can also be explicitly modeled in the same description. VHDL enable us to express the concurrent or sequential behavior of a digital system with or without timing. It also allows us to model the system as an interconnection of components.

IV. CONCLUSION

The main focus of this paper is to introduce a method for calculating the linear convolution, circular convolution and deconvolution with the help of vedic algorithms that is easy to learn and perform. The execution time and area of the proposed method for convolution using vedic multiplication algorithm is compared with that of convolution with the simple multiplication is less. From the simulated results it is observed that delay of Linear Convolution architecture is reduced by approximately 88% than the conventional method. An extension of the proposed linear convolution approach to circular convolution using vedic multiplier is also introduced which has less delay and area than the conventional method. This paper also introduced a straightforward approach to performing the deconvolution.

REFERENCES

[1] Surabhi Jain and Sandeep Saini , Electronics and Communication Department"High Speed Convolution and Deconvolution Algorithm based on ancient Indian vedic mathematics "

[2] G.Ramanjaneya Reddy and A. Srinivasulu ,Srinivasa Institute of Tech & Sci, Kadapa, GITAM University, Banglore campus , India " An Efficient Method for Implementation of Convolution"

[3] Madhura Tilak ,"An Area Efficient, High Speed Novel VHDL Implementation of Linear Convolution of Two Finite Length Sequences Using Vedic Mathematics"

[4] Asmita Haveliya, M.Tech. (Pursuing), Dept. Of Electronics, ASET Amity University Lucknow, India."FPGA IMPLEMENTATION OF A VEDIC CONVOLUTION ALGORITHM"

[5] Abdulqadir Alaqeeli and Janusz Starzyk [4], Ohio University School of Electrical Engineering and Computer Science "Hardware Implementation for Fast Convolution with a PN Code Using Field Programmable Gate Array"

[6] Rashmi K. Lomte (Mrs.Rashmi R. Kulkarni), Prof.Bhaskar P.C,"High Speed Convolution and Deconvolution Using Urdhva Triyagbhyam." VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on. IEEE, 2011.

[7] Mrs.Rashmi Rahul Kulkarni , (Electronics and Telecommunication, Finolex Academy of Management and
Technology/Mumbai University, INDIA) "Parallel Hardware Implementation of Convolution using Vedic Mathematics"

[8] J. G. Proakis and D. G. Manolakis, "Digital Signal Processing: Principles,Algorithm, and Applications," 2nd Edition. New York Macmillan, 1992.

[9] Pierre, John W. "A novel method for calculating the convolution sum of two finite length sequences."
Education, IEEE Transactions on 39.1 (1996): 77-80.