Design of CMOS Schmitt Trigger

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Abstract—Portable electronic devices have extremely low power requirement to maximize the battery lifetime. Various device circuit architectural level techniques have been implemented to minimize the power consumption. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order). However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases.

CMOS Schmitt trigger design with given circuit thresholds is described. The approach is based on studying the transient from one stable state to another when the trigger is in linear operation. The trigger is subdivided into two sub circuits, each of them is considered as a passive load for the other. This allows the relations governing the deviations of the circuit thresholds from their given values to be obtained. The trigger device sizes are thus determined by the threshold tolerances. Two new Schmitt trigger designs were presented. As opposed to the traditional implementation scheme, the new design approach used two separate inverters for each positive feedback paths. This modification resulted in near independent trip point control by varying the sizing of the respective feedback inverter in the first proposed design. In the second proposed design, the feedback inverters where modified to include two inputs, one from the internal node of the Schmitt trigger and the other being the output node, which resulted in independent control of the trip points by the sizing of the respective two input inverters. Simulations for these structures showed wide trip point control by varying feedback inverters sizing, specifically by the latter modification utilizing two input inverter scheme. The proposed structures also have added advantage of reduced kick back noise. These structures can also have current sourcing and/or sinking voltage controlled transistors at the output of the input inverter, which can shift the hysteresis window without changing its width. Splitting of the inverters for separate feedback paths along with the use of two input inverters are not limited to the present architecture, but can be used in other Schmitt trigger designs making them more favorable to different applications.

Index Terms—BJT-bipolar junction transistor, CMOS complementary metal oxide semiconductor, LTP—lower trigger point, UTP—upper trigger point.

I. INTRODUCTION

This paper explores introduction of Schmitt trigger and it’s application. This chapter also explain motivation and objectiv.behind study of Schmitt trigger.

A Multivibrator

It is an electronic ckt. which having no, one or two stable states of operation and as per number of stable state it is classified into three types

1. Astable multivibrator
2. Monostable multivibrator
3. Bistable multivibrator

A.1 Bistable multivibrator

It has two stable states and by applying external input we can change existing state of output it is also called as a flip flop. Schmitt trigger is modified version of bistable multivibrator.

A.2 Schmitt trigger

Schmitt triggers are bistable networks that are widely used to enhance the immunity of a circuit to noise and disturbances. It is good as a noise rejecter. Schmitt trigger make use of waves, therefore it is widely used for converting analog signals into digital ones and to reshape sloppy, or distorted rectangular pulses. Hysteresis of the trigger eliminates noise making a cleaner and more reliable signal. The output of a Schmitt trigger changes state when a positive going input passes the upper trigger point (UTP) voltage and when negative going input passes the lower trigger point (LTP) voltage. The conventional Schmitt trigger has fixed hysteresis width.

The Schmitt trigger circuit is widely used in analog and digital circuit as wave shaping circuit to solve the noise problem. Beside that this circuit is widely design in various styles in order to drive the load with fast switching low power dissipation and low-supply voltage. Conventional Schmitt Trigger is shown in Figure 1 where the switching thresholds are dependent on the ratio of NMOS and PMOS. However this circuit will exhibit racing phenomena after the transition starts. Therefore in this paper we proposed CMOS Schmitt Trigger circuit which is capable to operate in low voltages (0.8V-1.5V), less propagation delay and stable hysteresis width.

Fig. 1 CMOS Schmitt trigger design

B Motivation

Schmitt triggers is electronic comparators that are widely used to enhance the immunity of circuits to noise and disturbances and are inherent components of various emerging applications. The main difference between Schmitt triggers and comparators lies in the DC transfer characteristics. The comparator shows only one switching threshold, while Schmitt trigger shows different switching thresholds for positive-going and negative-going input signals. This characteristic is called hysteresis. If the noise magnitude of the input signal is less than the switching threshold difference, Schmitt trigger will not respond, thus making Schmitt trigger immune to the undesired
noise. The Schmitt trigger is a circuit that converts a varying voltage into a stable logical signal (one or zero). The DC transfer characteristic needs hysteresis to reduce the sensitivity to noise and disturbances. The hysteresis in a Schmitt trigger offers better noise margin and noise stable operation. With proliferation of portable devices, low power circuits are extremely desirable.

C. Objective and scope of study

In this paper the scope of the CMOS Schmitt trigger design because of following reasons

MOSFETS consume less power in the driver circuit.
MOSFETS have greater bandwidth
MOSFETS are thermally more stable.
MOSFETS are considerably ‘faster’ than BJT’s.

II. LITERATURE SURVEY

This section explores previous work done in Schmitt trigger circuit. It also focuses on development in this field. It explain that the design is both old & new from experiment done on this logic.

A. Work done in CMOS Schmitt trigger

Low voltage adjustable CMOS Schmitt trigger using dynamic threshold MOS (DTMOS). Cross-coupled inverter with body control is employed to speed up the switching process, and control the intensity of the feedback. The proposed Schmitt trigger has been designed using 0.18 μm 0.4 V CMOS technology and analyzed using PSPICE with BSIM3V3 device models. The simulation results show rail-to-rail operation and independently adjustable switching voltages for both low-to-high (VT(LH)) and high-to-low (VT(HL)) as high as 15% of the supply voltage. The power dissipation is 0.13 μW.

CMOS Schmitt trigger design with given circuit thresholds is described. The approach is based on studying the transient from one stable state to another when the trigger is in linear operation. The triggers subdivided into two sub circuits; each of them is considered as a passive load for the other. This allows the relations governing the deviations of the circuit thresholds from their given values to be obtained. The trigger device sizes are thus determined by the threshold tolerances. Publish in January 1994 IEEE(2)

![Fig.2: CMOS Schmitt trigger and its transfer characteristic](image)

Comparison among various Schmitt triggers on the basis of their hysteresis width and average power consumed. Hysteresis width is improved by using two feedback loops as compared to conventional CMOS Schmitt trigger whose hysteresis width is fixed. All Schmitt trigger circuits have been realized using .25μm and .18μm CMOS technology and simulation results are presented in July 2012 IJEIT (3) Effect of W/L Ratio of Various Transistors on Hysteresis Curve. A) Typical Case, B) When W/L of M4 Increases, C) When W/L of M1 Increase, D) When W/L of M3 Increase, E) When W/L of M6 Increase

![Fig.3: Effect of W/L Ratio of Various Transistors on Hysteresis Curve](image)

Transistors on Hysteresis Curve

Sub-threshold operation holds promise for ultra low energy operation in emerging applications. Sub threshold operation is attractive for mid to high performance applications where power has become a limiting constraint. This paper proposes a low power Schmitt-Trigger using CMOS standard cell logic. Experimental results reveal that proposed design has reduced power consumption and has temperature sustainability. The paper also presents the application of Schmitt Trigger in SRAM. The simulation work has been done on Tanner EDA tool at 45nm technology presented by RTCCE 2013(4)

Schmitt triggers are commonly used in communication and signal processing techniques to solve noise problem. A low voltage Schmitt trigger circuit with tunable hysteresis is proposed in this paper. For obtaining hysteresis under low voltage, a cross-coupled static inverter pair is used. By adjusting the symmetrical load operation, the hysteresis of the Schmitt trigger is varied. The cross-coupled inverter pair regenerative operation is controlled by it. Designed in 0.18 μm CMOS process technology, the simulation results show that the proposed Schmitt trigger circuit’s triggering voltage can be adjusted approximately 0.5 V to 1.2 V. The proposed design is suitable to be implemented in buffers, sub-threshold SRAMs, retinal focal plane sensors, wireless transponders and pulse width modulation circuits. publish in 2013, ISSN (5)
III Working Of Cmos Schmitt Trigger

In this section, design of Schmitt trigger which covers transient as well as dc analysis. Effect of W/L on hysteresis curve will also be discussed. The Schmitt circuit is a general inverter circuitry (double transistor inverter) with two extra transistors for providing the hysteresis.

![Fig. 4 working of CMOS Schmitt trigger](Image)

The double transistor inverter is used because the transistors (M2 and M5) have some higher threshold voltage than M1 and M4 due to body bias effect and due to which the output switches to high from low or low from high when after the ON condition of M2 or M4 respectively. Now after addition of two more transistors M6 and M3 the circuit is capable to provide hysteresis. When zero input voltage is applied at the input, both M1 and M2 are in OFF condition while M4 and M5 are in ON condition and output is at high logic level. When the input reaches to threshold voltage of M1 transistor then M1 will be on, while M2 remains OFF and at this time output will be high M3 will be on, so M1 Try to pull down the node between M1 and M2 while M3 try to pull up this node to voltage VDD-VTH , so transistor M2 stays the output to HIGH logic level, now when the input rises up to the threshold voltage of M2 then output switches to low logic level, so effectively our switching point shifted to higher voltage referred as VIH. Similar in case when input is falling from higher logic level then PMOS’s comes into picture and switching point at output is shifted to some lower voltage referred as VIL. The difference between the VIH and VIL is referred as HYSTERESIS voltage. This refers to an extra amount of voltage added to low logic level at output or subtracted to high logic level at output, the output logic level’s will remain same. Similar in case when input is falling from higher logic level then PMOS’s comes into picture and switching point at output is shifted to some lower voltage referred as VIH. The difference between the VIH and VIL is referred as HYSTERESIS voltage. This refers to an extra amount of voltage added to low logic level at output or subtracted to high logic level at output, the output logic level’s will remain same. If we examine the conditions from transistors (M1, M2, M3).When output switches from high to low just before that: M2 in off condition,M1 and M3 in saturation condition.

IV PROPOSED SYSTEM

A Traditionally, the goal of CMOS circuit designers has been to obtain the best trade-off between delay and power consumption. As CMOS technology continues to scale towards the nanometer regime, millions of transistors are densely packed to increase the system functionality. Such advancements of dense packaging and shrinking device sizes led to the advent of further challenges in power density, leakage power, parametric yield, and process parameter variations. Furthermore, performance degradation of circuits due to leakage, poor noise margins, dense packaging results. B Mathematical Expression for CMOS Schmitt trigger:

\[
\text{VIL} = \beta_4 \beta_6 (VDD - VTH) \beta_4 \beta_6 \\
\text{VIH} = [VDD + \beta_1 \beta_3 VTH] / 1 + \beta_1 \beta_3
\]

C Hysteresis width:

Increasing of load capacitance will increase the hysteresis width (in small amount) for all three designs. Thus, the three designs are said to be stable at variation of load capacitance. \(\Delta H = VTH - VTL\). At VDD = 0.8V, While at VDD > 0.8V All the designs give a few mV hysteresis width, thus it is neither too wide nor too small for a Schmitt Trigger.

D Energy-delay product

The Energy-Delay Product (EDP) is measured using equation and theoretically EDP is directly proportional to Power-Delay Product (PDP) and propagation delay. EDP = CLV2DD t P = PDP x t P EDP also increases. The Proposed circuit give less EDP as low voltages (<1.2V) and low load capacitance (<0.015pF) due to less delay as discussed in section A. While at higher voltages (>1.0V) and high load capacitance (>0.010pF), the 1st Design gives the less EDP. As for the 2nd Design, it gives the highest EDP and thus is not preferably in a Schmitt Trigger.

V EXPERIMENTAL RESULTS

A SIMULATION RESULTS

The designs of CMOS Schmitt trigger is simulated with CMOS 65nmrule&CMOS 90nmrule foundry using Micro wind software. The layout design in microwind as shown in fig.5 and fig.8 for 90nm and 65nm technology as shown in below. In this ckt. The Vdd supply of 12v is required. Sinusoidal waveform input is applied. The size of PMOS is twice of size of NMOS. By following design rule the ckt. Of schmitt trigger is design. Different output of Schmitt trigger as shown in fig 6,7,8 9 for 90nm. And for 65nm shown in fig.10,11etc.

![Fig.5 Schmitt trigger design in Microwind for 90nm](Image)
VI. ADVANTAGES AND APPLICATIONS

A advantages
The CMOS Schmitt trigger has the following advantages

- High impedance input (1012 typical)
- Balanced input and output characteristics
- Thresholds are typically symmetrical to 1/2 VCC
- Outputs source and sink equal currents
- Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3V–15V), split supplies possible
• Low power consumption, even during transitions
• High noise immunity. 0.70 VCC typical

B Applications of the CMOS Schmitt trigger:
Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

1. The circuit in Figure 12 is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies. This biases the mean threshold value around zero an coupling from an opamp output possible.

![Fig. 12 sine to square wave converter](image)

In Figure 13 we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2. Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage. Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level.

![Fig.13. CMOS Schmitt Trigger Ignores Noise](image)

CONCLUSION
The design of a CMOS Schmitt trigger can be completed if the detailed circuit operation near the transition points is analyzed. This analysis gives true thresholds and allows one to evaluate the difference between the thresholds and the initial points of transitions (which are incorrectly considered and specified as thresholds). The voltage-current characteristics of the trigger sub circuits allow one to specify the conditions to make the trigger transfer characteristic more rectangular. The analysis is valid if the fabrication technology allows using the square-law characteristics of MOS devices.

REFERENCES