An Analytical Approach for Simulated IEEE 802.11(A) WLAN Standard Using Frequency Synthesizer

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***Abstract*— In wireless medium, requirement of high frequency is increasing day by day. For high frequency based system data rates should be high. In unguided media, as signal travels a long distance and due to interference of noise, there is error in phase and frequency and we get a deviated output. In view of this, We are motivated to design a low power frequency synthesizer which would provide a low locking time, low settling time, moderate value of damping factor to provide a efficient frequency response at the output end. The proposed design aspect is for high frequency which is implemented in IEEE 802.11(a) WLAN standard and OFDM technology, WCDMA, Bluetooth technology, high frequency processor. We have used Microwind 3.1 45nm technology and ADS as design tool to execute propose design.**

Keywords- Frequency synthesizer, phase frequency detector, voltage-controlled oscillators, Multi module divider,Microwind 3.1, ADS,wireless communication.

I. INTRODUCTION

The demand for high data rate wireless local area networks (WLANs),High frequency processor with low power consumption is rapidly increasing. The unlicensed national information infrastructure (UNII) band provides 300MHz of spectrum at 5GHz for wireless communications. The lower 200MHz of this band overlaps the high performance radio LAN (HIPERLAN) frequency band. This frequency band is divided into 8 channels. In this paper we examine the design of a fully integrated frequency synthesizer as a local oscillator (LO). We also demonstrate the advantage of a voltage controlled differential injection locked frequency divider (VCDILFD) as a low power frequency divider in this high frequency synthesizer[1]. The Frequency synthesizer invented in the earlier years for reduction of the noise in the radio received signal was observed that the signal coming from the distance source is producing some noise if it is not properly tuned and latter it observed that the noise is produced due to mismatch of phase and frequency at the receiver input and a circuit was designed to reduce the phase and frequency error at the receiver side .With the time passes the frequency of operation increases and the requirement of fast loop locking is required. This aspect motivated us to design a frequency synthesizer for high frequency application. In this paper, new techniques and architectures are presented and developed to address those challenges. First, a low-phase-noise ring oscillator and a capacitor multiplier with a high-multiplication factor efficiently minimize the silicon area of sub-components, and a compact programmable delay-locked loop (DLL)-based frequency multiplier is developed to replace the PLL-based frequency synthesizer. Second, the charge-distribution mechanism for suppressing reference spurs is theoretically analyzed[2], and an edge interpolation technique for implementing the mechanism is developed. Finally, the concept and the architecture of sub-integer-N PLL is proposed and implemented to remove trade-offs between conventional integer-N PLLs and fractional-N PLLs.

SYSTEM ARCHITECTURE

Block diagram

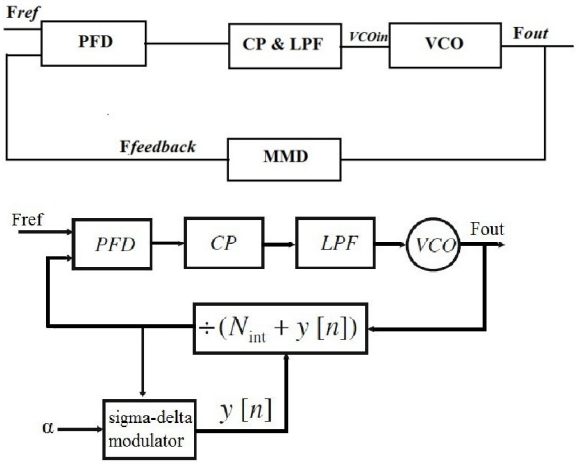

Figure 1. Block diagram of frequency synthesizer.

Description

Frequency synthesizer is circuit which synthesizes and generates a clock for the prescribed frequency. It uses a negative feedback to correct phase and frequency of signal so that whatever signal get recovered should be error free. Frequency multiplier which multiplies by a factor to low frequency input F_{ref} to convert it into higher frequency output $F_{out.}$

The main purpose of this frequency synthesizer block is to recover the signal without phase and frequency error.

Main block of frequency synthesizer is

- Phase frequency detector
- Charging pump
- Low pass filter
- VCO
- Multi module divider

Phase frequency detector

The first block of PLL circuit is PFD, which is used for detecting the frequency with reference frequency. The basic function of a PD or a PFD is to detect the difference in the phase or frequency between two incoming signals-the reference clock and the divided VCO clock-and to deliver the information to the subsequent CP[7]. PDs can be broadly classified into two topologies: the multiplier type and the sequential type. The multiplier-type PD generates a DC error output as the average product of the reference clock and the divided VCO clock. The sequential-type PD generates the output signal purely as a function of the time interval between two incoming clocks, so the sequential-type PD contains the memory of past transitions. Among sequential-type PDs, the tri-state PFD is one of the most

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common topologies to be utilized with a CP, as in Figure 2. As its name implies, the tri-state PFD can take one of three states. When the phase and frequency differences between the reference clock and the divided VCO clock are detected, the tri-state PFD generates two output signals. The UP and the DN, to convey the information. By rising edges of the reference clock, *fref*, and the divided VCO clock, *fdiv*, the UP and the DN become 1 simultaneously.

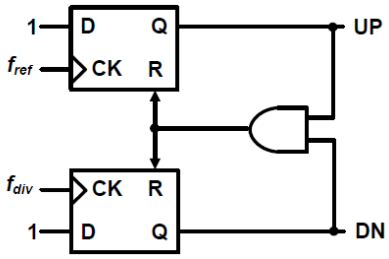

Figure 2. Block diagram of phase frequency detector.

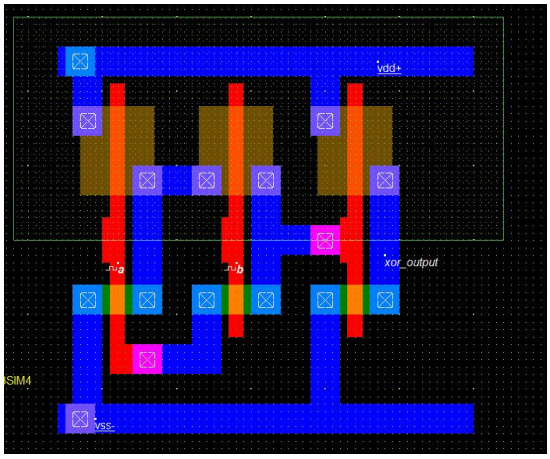

Figure 3. CMOS layout of phase detector

Charging pump

The phase/frequency difference information conveyed in the pulse width of the output signals of the PFD should be converted into the form of DC voltage in order to modulate the output frequency of the VCO. Generally, this time-to-voltage conversion process takes place through the charge pump and the loop filter, as shown in Figure. First, the charge pump converts the pulse-modulated phase/frequency difference information into corresponding charges, and then these charges are translated to DC voltage by the loop filter.

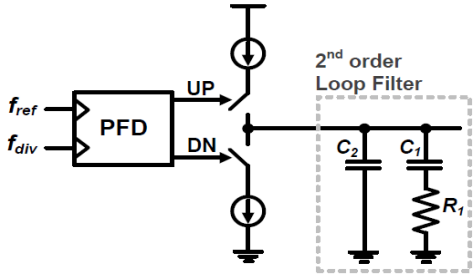

Figure 4. Block diagram of charge pump and second order loop filter.

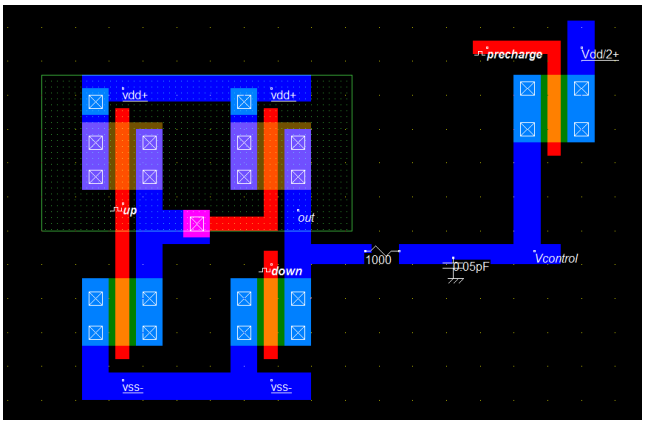

Figure 5. CMOS Layout of charge pump and loop filter

Loop Filter

The Filtering operation of the error voltage (coming out from the Phase Detector) is performed by the loop filter. The output of PD consists of a dc component superimposed with an ac component. The ac part is undesired as an input to the VCO, hence a low pass filter is used to filter out the ac component. Loop filter is one of the most important functional block in determining the performance of the loop. A loop filter introduces poles to the PLL transfer function, which in turn is a parameter in determining the bandwidth of the PLL[9]. Since higher order loop filter is define over better noise cancelation, a loop filter of order 2 or more is used in most of the critical application PLL circuits. If the PFD output is Q_a high for time Δt in that case the total phase error at the output of the PFD is

$$\Delta\varphi=\Delta t/T_{clock}*2\Pi(\text{radian}) \qquad (1)$$

Where is the phase error of the two input at PFD and the value of phase error are given in radians and the value of output voltage of charge pump is

$$V_{\text{charge pump}} = \{(V_{DD}-0)/4\Pi\}*\Delta\varphi= K_{cp}*\Delta\varphi \qquad (2)$$

Voltage-Controlled Oscillator

To enhance the phase noise performance of a ring VCO, the proposed ring VCO adopts the saturated type delay cell of with a cross-coupled latch. Thus, the delay cell eliminates the tail current source and has pseudo-differential configuration using a PMOS cross-coupled latch. As a saturated-type VCO, the delay cell allows a rail-to-rail output signal swing. In addition, the cross-coupled latch accelerates the signal and provides fast-switching edges. When the signal is injected, the latch operates in the direction of opposing the signal transition in the PMOSs. However, after a while, the function of the latch changes into a positive feedback and accelerates the signal transition. With the rail-to-rail swing signal with fast-switching transition, the proposed oscillator can enhance phase noise performance compared to conventional ones.[20]

A typical example of an unturned oscillator is a ring oscillator. The ring VCOs without inductors can be implemented in a small die area. Thus, in this work, a ring type oscillator has been considered in order to integrate a VCO

generating quadrature output signals for the SSB mixer in compact chip area for improving the poor phase noise performance the proposed oscillator adopted a saturated-type delay cell with a latch configuration. The schematics of the proposed delay cell and the 3-stage ring oscillator are shown in Figure,

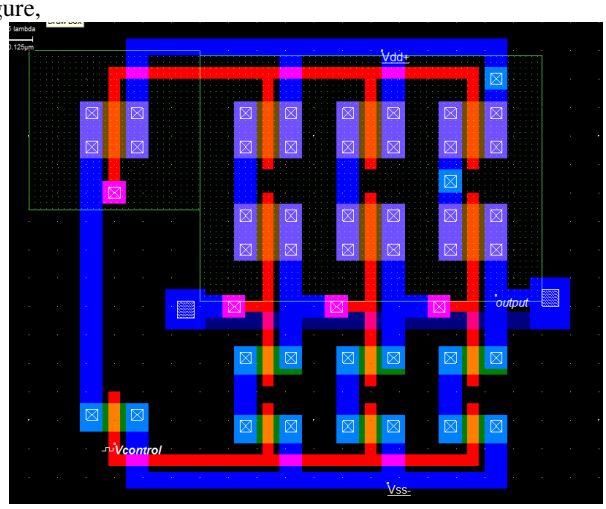

Figure 6. Diagram of three stage ring oscillator.

Multi-Modulus Divider

The multi-modulus divider is a programmable architecture of generic chain divider in which one divider is connected to other in the cascaded manner so that every divider divides the output of the previous divider in a controlled way of division. [10]

The multi-modulus divider is a programmable architecture of generic chain of N/N+1 divider in which one divider is connected to other in the cascaded manner so that every divider divides the output of the previous divider in a controlled way of division. The N/N+1 divider represent here as the 2/3 divider in which the same divider circuit divide the input either by 2 or by 3 depending upon the programmable input of the divider. The 2/3 divider circuit is the combination of four D-latch which are arranged by the combination of AND gate and NOT gate with them in which the input frequency is given to the clock point in each latch

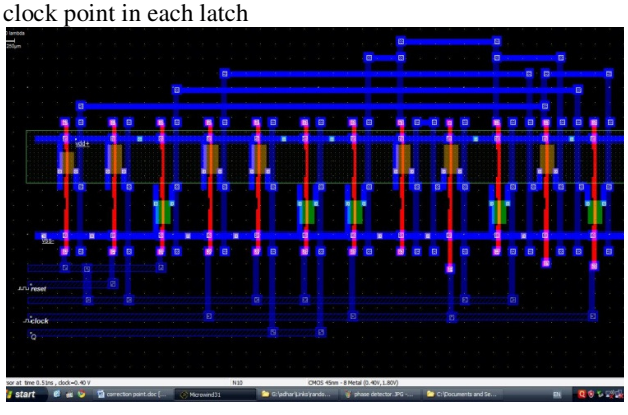

Figure 7. Block diagram of Multi module divider.

Frequency synthesizer in ADS

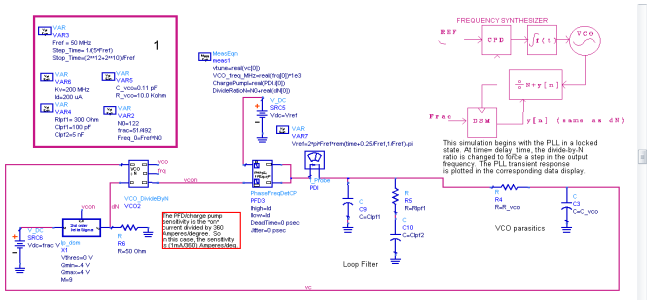

Figure 8. Complete architecture of frequency synthesizer in ADS tool

II. NOISE IN FREQUENCY SYNTHESIZER

The output of the practical system deviates from the desired response. This is because of the imperfections and noises in the system. The supply noise also affects the output noise of the frequency synthesizer system. There are mainly two types of noises. They are explained below.

Phase Noise and jitter

This paper presents a comprehensive analysis of jitter and phase noise in both CMOS inverter based and differential ring oscillators, pinpointing the most important mechanisms whereby white and flicker noise manifest themselves. The physically based approach and simple resulting expressions should make it easy to design ring oscillators for a given jitter. In fact, these simple expressions predict jitter and phase noise much more accurately than oscillation frequency; this is similar to what is seen in amplifier design, where input-referred noise is predicted much more accurately than gain [12].

A jitter is a variation of the reference signal with respect to ideal position in time. Jitter and phase noise is related to each other and by calculating one you can get the idea about other. The jitter impacts the data transmission quality. The deviation of the signal from the ideal position can cause the increases in bit error rate (BER) of communication signal.

III. PARAMETER IN FREQUENCY SYNTHESIZER

Rise time

The rise time is the time taken by the output to reach from 10% to 90% of the final value of the output and it is controlled by the damping ratio of the low pass filter.

Peak overshoot

In the case of under damped system at the first instance when the transient overshoot occur over the settled value is known as the peak overshoot normally in the circuit the under damped system provide a fast output response but due to high peak overshoot it may damage the output response of the circuit so that the peak overshoot must be within some reasonable value.

Lock time

The minimum time required for a frequency synthesizer to get locked is known as the lock in time .after this time the frequency synthesizer is locked permanently to the fix output frequency.

Pull-in time

This is the time required to pull in the signal in the fast locking state when the signal are locking or acquisition time is very slow .once the signal comes in the fast locking state then it will lock very fast. Generally pull-in process is slow.

IV. RESULT ANALYSIS OF SYNTHESIZER

Phase frequency detector

The state of PFD is determined by the positive edge transitions on the inputs an as shown in the state diagram. If the phase is same it will show the constant steady output. If the phase is different it will show the output with phase difference.

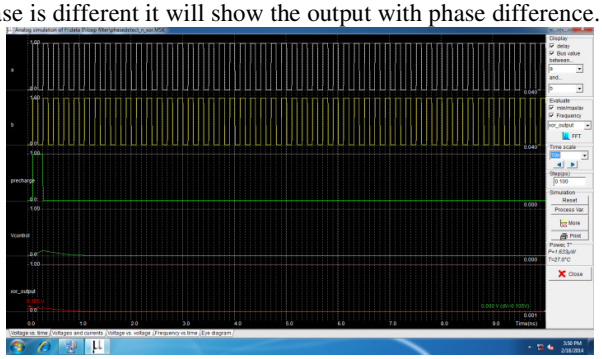

Figure 9. The outputs of PFD when phase is same

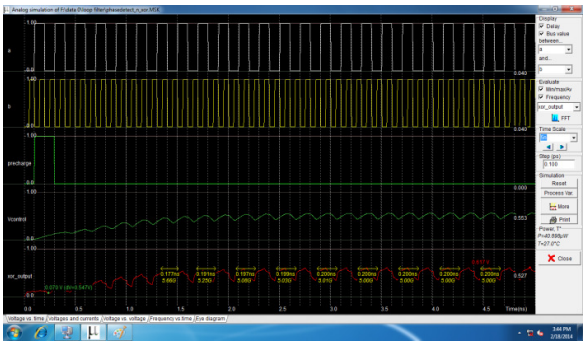

Figure 10. The outputs of PFD when phase is different

Charge Pump and loop filter

The output of a PFD can be converted to DC (voltage/current) in many different ways. One approach is to sense the difference between the two outputs by using a differential amplifier and apply the result to a low pass filter. Calculation of various parameters in the circuit is done through the dynamic response of the control voltage which is actually an output of the second order closed loop system so that the calculation is done with this response. From below figure we can see that the circuit is producing an overshoot at some point of time so that from that figure take the value of maximum over shoot and also calculate the peak time on which the maximum overshoot is coming. By taking this two value calculate the value of damping ratio and natural frequency of oscillation[15]

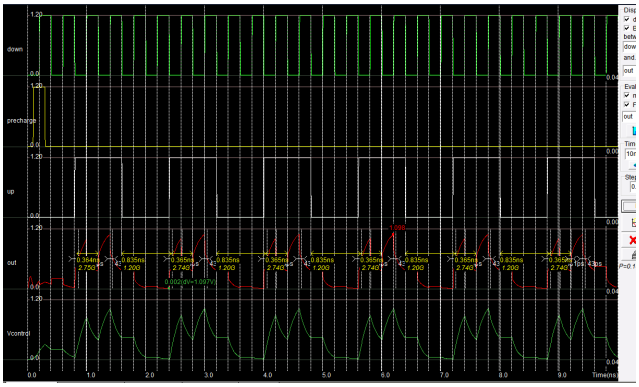

Figure 11. The outputs of Loop filter

Voltage controlled oscillator

The voltage controlled oscillator is a 5 stage current starved voltage controlled oscillator that is oscillating at the frequency of 17GHz as the centre frequency[18]. The centre frequency in this VCO is obtained at the controlled voltage of $V_{DD}/2$.The V_{DD} in this circuit 1.2 volt so the centre frequency is obtained at the controlled voltage.[20]

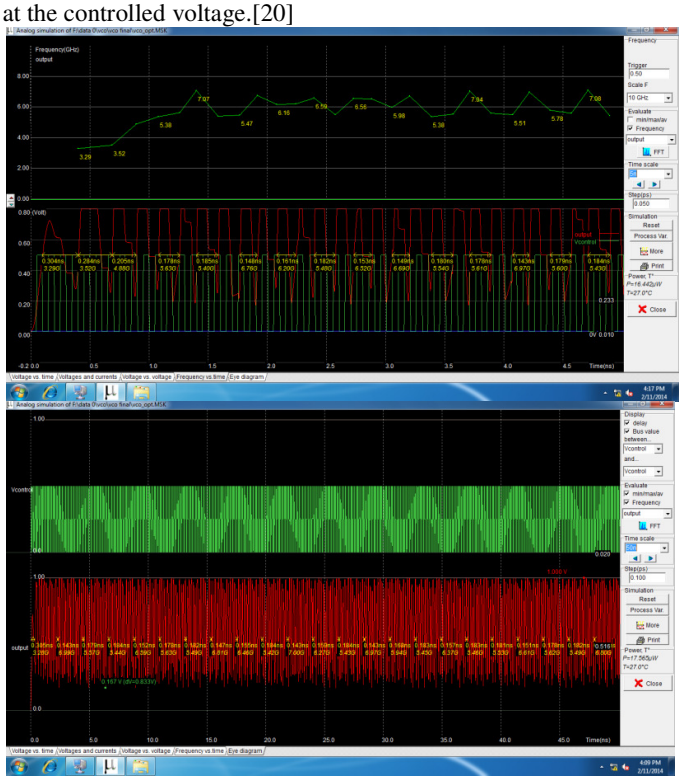

Figure 12. The ouput frequency of Ring Oscillator

Multi module divider

In the prapose architecture we have design the MMD which can divide the clock by 2 with falling edge

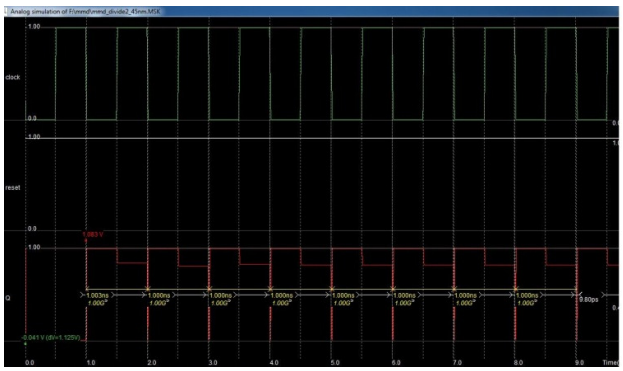

Figure 13. Ouput of MMD

CONCLUSION

A 6 GHz fully integrated frequency synthesizer is presented. The phase frequency detector decides the linearity and the pull-in range of the frequency synthesizer therefore the selection of PFD is very important in the design. For fractional frequency divider the design of divider circuit is very important and it further decides the range of frequency which can be applied to the frequency synthesizer.

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